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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/978,528	10/17/2001	Andres Bryant	BU9-99-055	5054

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/978,528	BRYANT ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25 and 27-33* is/are pending in the application.

4a) Of the above claim(s) *1-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-25 and 27-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on January 9, 2004 has been entered; no new claims have been added.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 23-25 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deleonibus USPN 6,091,076 in view of Koh USPN 6,049,110.

Deleonibus discloses in figs. 1 and 2 a semiconductor device comprising a semiconductor layer formed on an insulating layer 44; a gate conductor 20 formed on the semiconductor layer; spacers 24/26 formed on sidewalls of the gate conductor and on the semiconductor layer; extension regions 8, 10 extending further under the spacers than diffusion regions 4, 6 (as in claim 28) arranged in the semiconductor layer on both sides of the gate conductor and extending at least under the spacers; diffusion regions 4, 6 formed in the semiconductor material adjacent to the extension regions such that a portion of at least one of the extensions regions is exposed at a surface of the semiconductor layer; and a metal layer 12/14 contacting the diffusion region (as in claim 25) formed at least in the exposed portion of the extension region, the metal layer contacting the semiconductor layer, but does not disclose extension regions extending and contacting said spacer and a portion of said gate conductor.

Koh discloses in fig. 43 a semiconductor device comprising a semiconductor layer formed on an insulating layer 31 including extension regions (regions under reference numerals 55 and 56) extending further under the spacers 55 arranged in the semiconductor layer on both sides of a gate conductor 56 and extending under and contacting the spacers and a portion of the gate conductor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Koh's teachings with Deleonibus' device since that would suppress short channel effects as taught by Koh.

As to claim 24, Deleonibus discloses extension regions lower doped than the diffusion regions.

As to claim 27, Deleonibus discloses extension region exposed on both sides of the gate conductor and the metal layer formed in both the exposed portions of the extension regions.

As to claim 29, Deleonibus discloses said metal layer and said exposed portion of the extension region form an schottky diode.

4. Claims 23-25 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. ("Yamaguchi") USPN 5,341,028 in view of Imai USPN 6,297,529 and Koh USPN 6,049,110.

Yamaguchi discloses in figs. 5 and 6 a semiconductor device comprising a semiconductor layer formed on an insulating layer 12; a gate conductor 20 formed on the semiconductor layer; spacers 25/26 formed on sidewalls of the gate conductor and on the semiconductor layer; extension regions 15, 16 extending further under the spacers than diffusion regions 17, 18 (as in claim 28) arranged in the semiconductor layer on both sides of the gate

conductor and extending at least under the spacers; diffusion regions 17, 18 formed in the semiconductor material adjacent to the extension regions such that a portion of at least one of the extensions regions is exposed at a surface of the semiconductor layer; a metal layer 27 contacting the diffusion region (as in claim 25) formed at least in the exposed portion of the extension region, but do not disclose said extension regions extending and contacting said spacer and a portion of said gate conductor or said metal layer contacting the semiconductor layer.

Imai discloses in fig. 2 a semiconductor device comprising a semiconductor layer 5/6; a gate conductor 14; extension regions 16 extending further under spacers 17 than diffusion regions 19 arranged in the semiconductor layer on both sides of the gate conductor and extending at least under the spacers; and a metal layer 20 formed at least in the exposed portion of the extension region and extending into the semiconductor layer (as in claim 30) or extends into a portion of the semiconductor layer below said extension region (as in claim 31), the metal layer contacting the semiconductor layer.

Koh discloses in fig. 43 a semiconductor device comprising a semiconductor layer formed on an insulating layer 31 including extension regions (regions under reference numerals 55 and 56) extending further under the spacers 55 arranged in the semiconductor layer on both sides of a gate conductor 56 and extending under and contacting the spacers and a portion of the gate conductor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Imai's teachings with Yamaguchi's device since that would prevent an increase of the contact resistance of the gate electrode with the metal layer. It would have been

obvious to incorporate Koh's teachings since that would suppress short channel effects as taught by Koh.

As to claim 24, Yamaguchi discloses extension regions lower doped than the diffusion regions.

As to claim 27, Yamaguchi discloses extension region exposed on both sides of the gate conductor and the metal layer formed in both the exposed portions of the extension regions.

As to claim 29, Yamaguchi discloses said metal layer and said exposed portion of the extension region form an schottky diode.

5. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. ("Yamaguchi") USPN 5,341,028 in view of Gardner et al. ("Gardner") USPN 6,096,615 and Koh USPN 6,049,110.

Yamaguchi discloses in figs. 5 and 6 an integrated circuit disposed on an SOI substrate having a body region 14, comprising a transistor having a source diffusion region 17, a gate formed over said body region, a first sidewall spacer disposed on a side wall of said gate abutting said source diffusion region, a drain diffusion region 18, a second sidewall spacer disposed on a side wall of said gate abutting said drain diffusion region, and extension diffusion regions that extend further under said gate than said source diffusion region or said drain diffusion region, said extension diffusion regions having a dopant concentration less than that of said source diffusion region and said drain diffusion region; and a conductor 27 in contact with a portion of said extension regions and a portion of source diffusion region to form a Schottky contact diode that prevents charge from accumulating in said body region, but do not disclose extension diffusion regions provided under and contacting first and second sidewall spacers, said extension

diffusion regions contacting said gate and extending further under the gate or a first sidewall spacer thinner than a second sidewall spacer.

Gardner discloses (see fig. 2G and col. 5, lines 1-15) an integrated circuit comprising a first sidewall spacer 210 thinner than a second sidewall spacer 219.

Koh discloses in fig. 43 a semiconductor device comprising a semiconductor layer formed on an insulating layer 31 including extension diffusion regions (regions under reference numerals 55 and 56) provided under and contacting first and second sidewall spacers 55, said extension diffusion regions contacting said gate and extending further under the gate conductor 56 and extending further under said gate conductor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Gardner's teachings since that would be useful in subsequent dopant implant step as taught by Gardner. It would have been obvious to incorporate Koh's teachings since that would suppress short channel effects as taught by Koh.

6. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi in view of Gardner and Koh as applied to claim 32 above, and further in view of Imai USPN 6,297,529.

The combined references disclose the device structure as recited in the claim, but fail to disclose a conductor in contact with a body region.

Imai discloses in fig. 2 an integrated circuit having a body region 5/6; a gate conductor 14; extension regions 16 extending further under spacers 17 than diffusion regions 19 arranged in the semiconductor layer on both sides of the gate conductor and extending at least under the spacers; and a conductor 20 contacting the body region.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Imai's teachings since that would prevent an increase of the contact resistance of the gate electrode with the conductor layer.

7. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deleonibus USPN 6,091,076. in view of Gardner et al. ("Gardner") USPN 6,096,615 and Koh USPN 6,049,110.

Deleonibus discloses in fig. 2 an integrated circuit disposed on an SOI substrate having a body region 42, comprising a transistor having a source diffusion region 4, a gate 20 formed over said body region, a first sidewall spacer 20 disposed on a side wall of said gate abutting said source diffusion region, a drain diffusion region 6, a second sidewall spacer 26 disposed on a side wall of said gate abutting said drain diffusion region, and extension diffusion regions that extend further under said gate than said source diffusion region or said drain diffusion region, said extension diffusion regions having a dopant concentration less than that of said source diffusion region and said drain diffusion region; and a conductor 12/14 in contact with a portion of said extension regions and a portion of source diffusion region to form a Schottky contact diode that prevents charge from accumulating in said body region, but do not disclose extension diffusion regions provided under and contacting first and second sidewall spacers, said extension diffusion regions contacting said gate and extending further under the gate or a first sidewall spacer thinner than a second sidewall spacer.

Gardner discloses (see fig. 2G and col. 5, lines 1-15) an integrated circuit comprising a first sidewall spacer 210 thinner than a second sidewall spacer 219.

Koh discloses in fig. 43 a semiconductor device comprising a semiconductor layer formed on an insulating layer 31 including extension regions (regions under reference numerals 55 and 56) extending further under the spacers 55 arranged in the semiconductor layer on both sides of a gate conductor 56 and extending under and contacting the spacers and a portion of the gate conductor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Gardner's teachings with Deleonibus' device since that would be useful in subsequent dopant implant step as taught by Gardner. It would have been obvious to incorporate Koh's teachings since that would suppress short channel effects as taught by Koh.

8. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deleonibus in view of Gardner and Koh as applied to claim 32 above, and further in view of Imai USPN 6,297,529.

The combined references disclose the device structure as recited in the claim, but fail to disclose a conductor in contact with a body region.

Imai discloses in fig. 2 an integrated circuit having a body region 5/6; a gate conductor 14; extension regions 16 extending further under spacers 17 than diffusion regions 19 arranged in the semiconductor layer on both sides of the gate conductor and extending at least under the spacers; and a conductor 20 contacting the body region.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Imai's teachings since that would prevent an increase of the contact resistance of the gate electrode with the conductor layer.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hause et al. USPN 6,255,703 disclose a semiconductor device with lower LDD resistance.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

ANS
April 7, 2004